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In the present invention, the virtual address is composed of a segment *identifier*, which is converted by a segmentation process or apparatus, into a linear address. In the present invention, the virtual address is composed of a segment identifier and a segment offset, which is converted by a segmentation process or apparatus into a linear address. In the present invention, during the virtual-to-linear translation, the segment offset contributes to the both the page and word (or byte) offset of the linear address. This is characteristic of the two step (virtual-to-linear, then linear-to-real) independent segmentation and paging scheme of the environments where the present invention is used. There is no such separate segmentation process or apparatus disclosed or taught by Toy, because there is no such linear address. In Toy, the virtual address closely corresponds to the present invention's linear address, but there is no separate segmentation process or hardware to generate it.

Accordingly, we believe that Toy is easily distinguishable because it does not really teach or disclose either: (1) a virtual address of the [segment identifier: segment offset] variety; (2) a linear address of the type used in the present invention; or (3) a virtual-linear address conversion operation. Again, we think the claims already differentiate from such a system, but we have suggested some proposed amendments herein to clarify the scope of the present invention. These amendments track these distinctions fairly closely.

Please let me know at your earliest convenience whether you agree with these proposals. If so, I can get something to you next week by way of a formal amendment to formalize this approach. Should you have questions, or wish to discuss this in person further, please give me a time and date where we can set aside a few minutes to do so.

Very truly yours,

J. Nicholas Gross
Law+
34,175

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38. (Twice amended) A system for performing address translations **usable by a processor employing both segmentation and optional independent paging** [said system generating an actual physical address from a virtual address in a time period T, by calculating a linear address based on said virtual address, and by calculating said actual physical address based on said calculated linear address, said system further including] **the system** comprising:

means for generating an actual physical address from a virtual address in a time period T, **said virtual address having both a segment identifier and a segment offset** by calculating a linear address based on said **entire** virtual address, and by calculating said actual physical address based on said calculated linear address; and

a fast physical address generator for generating a fast physical address related to said virtual address in a time < T.

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43. (Amended) A system for performing address translations using a first operation to convert a first virtual address having both a segment identifier portion and a segment offset portion to a first linear address, the first lineat address being based on all portions of the virtual address and a second operation to convert said first lincar address to a first physical address, said system further including:

a tentative physical address generator for generating a tentative physical address related to said first virtual address;

wherein the tentative physical address can be generated before said second operation has completed converting said first linear address.

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49. (Amended) A computer system which performs [for performing] address translations using a first operation to convert virtual addresses having both a segment identifier portion and a segment offset portion to linear addresses, such that both the segment identifier and segment offset portions of the virtual addresses are used for converting said linear addresses and a second operation to convert said linear addresses to physical addresses, said system further including:

a fast physical address generator for generating fast physical addresses related to said virtual addresses;

wherein the fast physical addresses can be generated while said virtual addresses are being converted in said first operation into said linear addresses.

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54. (Amended) A system for performing address translations comprising:

a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address, said virtual address having both a segment identifier and a segment offset, and said calculated linear address being based on all of said virtual address; and

a linear to physical address converter circuit for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset;

wherein a memory reference can be generated based on the fast physical address.

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57. A system for performing address translations using a first operation to convert a first virtual address having both a segment identifier portion and a segment offset portion to a first linear address, such that all portions of the virtual address are considered when converting said virtual address into the first linear address and a second operation to convert said first linear address to a first physical address, the system further including:

an address translation memory, accessible by said system while said first operation is converting said first virtual address, and capable of storing prior physical address information generated during a prior address translation by said second operation based on a prior virtual address;

wherein a fast physical address can be generated based on the prior physical address information and said first linear address before said second operation has completed converting said first linear address.

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61. (Amended) A computer system using segmentation and optional independent paging for performing address translations comprising:

an address translation memory capable of storing:

(i) a portion of a physical address corresponding to a stored page frame; and

(ii) segment base information relating to a virtual address; and

a virtual to linear address converter circuit for generating a calculated linear address based on combining [a] segment offset portion of the virtual address and the segment base, wherein all of said virtual address is used for generating the calculated linear address; and

a linear to physical address converter circuit for receiving and generating a calculated physical address based on the calculated linear address, the calculated physical address including a first page frame and a first page offset; and

a fast physical address circuit for generating a fast physical address comprised of the stored page frame combined with a fast page offset portion derived from the segment base and the virtual address;

wherein the fast physical address is calculated prior to the generation of said calculated physical address.

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66. (Amended) A method of performing a translation of a virtual address in a computer system using segmentation and optional independent paging, said method including the steps of :

(a) calculating a fast physical address related to said virtual address; and

(b) calculating a linear address based on said virtual address, said linear address being based on both a segment identifier and segment offset portion of said virtual address; and

(c) calculating an actual physical address based on the linear address;

wherein step (a) is completed prior to the completion of step (c), and the fast physical address can be used to initiate a fast memory reference.

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70. (Amended) A method of generating memory references based on virtual addresses in a computer system, said computer system using segmentation and optional independent paging, the method including the steps of:

(a) generating tentative memory references based on said virtual addresses; and

(b) converting said virtual addresses to linear addresses during a segmentation operation, said linear addresses being based on translating all portions of said virtual address; and

(c) converting said linear addresses to physical addresses during a paging operation, so that actual memory references can be made based on said physical addresses;

wherein the tentative memory reference can be generated while said virtual addresses are being converted in said first operation into said linear addresses.

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74. (Amended) A method of generating a fast memory reference using a fast physical address derived from a virtual address having both a segment identifier and a segment offset in a computer system employing both segmentation and optional independent paging, the method including the steps of:

(a) converting a portion of said virtual address into a partial linear address; and

(b) combining the partial linear address with physical address information obtained from a prior memory reference to generate said fast physical address;

(c) generating a memory reference based on the fast physical address;

(d) converting said virtual address into an actual physical address during which time a linear address is also calculated based on both the <segment id> and <segment offset> of said virtual address;

(e) cancelling the memory reference if the fast physical address and actual physical address are different.

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77. (Amended) A method of generating physical addresses from virtual addresses in a computer system employing both segmentation and optional independent paging, the method including the steps of:

(a) generating a first calculated linear address based on a first virtual address in a first operation, said linear addresses being based on translating all portions of said first virtual address; and

(b) generating a fast physical address in a second operation, the fast physical address including linear address information relating to said first virtual address and portions of physical address information relating to said first virtual address; and

(c) generating a first calculated physical address in a third operation based on the first calculated linear address;

wherein the fast physical address is generated prior to the generation of the first calculated physical address.

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82. (Amended) A system for performing memory references in a processor which employs both segmentation and optional independent paging during an address translation, said system comprising:

means for performing an address translation by generating a first physical address from a first virtual address by first calculating a first linear address based on both a first segment identifier and first offset associated with the first virtual address, such that all of said first virtual address is translated, and then calculating the first physical address based on the first calculated linear address; and

a fast physical memory access circuit for generating a fast memory reference, which fast memory reference is based on physical address information from said address translation means;

a bus interface circuit for initiating a fast memory access to a memory subsystem based on said fast memory reference.

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86. (Amended) A method for performing memory accesses between a processor and a memory, said processor having an address translation mechanism that employs segmentation and optional independent paging, the method comprising the steps of:

generating computed physical addresses by converting virtual addresses having a segment identifier and a segment offset into linear addresses, such that all portions of said virtual addresses are translated, and then converting said linear addresses into a physical addresses;

generating a speculative physical address based on one of said computed physical addresses;

initiating a speculative memory access based on said speculative physical address.

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89. (Amended) A system for performing a first and a second address translation of first and second virtual addresses respectively, the system comprising:

a virtual to linear address converter circuit for generating a first calculated linear address based on translating all portions of the first virtual address including a segment identifier and a segment offset; and

a linear to physical address converter circuit for completing the first address translation by generating a first calculated physical address based on said first calculated linear address, said first calculated physical address including a first calculated page frame and a first calculated page offset; and

wherein the system uses information from the first address translation during the second address translation so that the second address translation can be performed faster than the first address translation.

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95. (Amended) A circuit for performing fast translations of virtual addresses to physical addresses in a computer system which uses both segmentation and optional independent paging, the circuit including:

an address generator for performing a first address translation of a first virtual address having an associated first segment identifier and a first offset, said first translation including converting all of said virtual address into a first linear address;

said address generator also performing a fast address translation of a second virtual address having an associated second segment identifier and a second offset, said fast address translation occurring without converting all of said second virtual address into a second linear address;

wherein said address generator uses information from the first address translation during the fast address translation so that said translation of said second virtual address takes less time than said first address translation.

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101. (Amended) A method of translating virtual addresses in a computer system that uses both segmentation and optional independent paging, the method including the steps of:

(a) generating a first calculated physical address based on a first virtual address in a first operation, said first virtual address including a first segment identifier and a first offset and wherein said first operation converts all of said virtual address into a first linear address; and

(b) generating a second fast physical address in a second operation based on a second virtual address, said second virtual address including a second segment identifier and a second offset, and said second fast physical address being generated based on information obtained during said first operation, and without converting all of said second virtual address into a second linear address;

wherein said second operation is performed faster than said first operation.

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107. (Amended) A method of performing address translations in a computer system that uses both segmentation and optional independent paging, the method including the steps of:

(a) performing a first address translation by translating a first virtual address into a first physical address by: (i) first calculating a first linear address based on a first segment identifier and first offset associated with said first virtual address wherein all of said virtual address is translated; and (ii) calculating said first physical address based on said first calculated linear address and

(b) performing a second address translation using information obtained during said first address translation to translate a second virtual address into a second physical address, said second physical address being obtained without converting all of said second virtual address into a second linear address;

wherein said second translation can be achieved in less time than said first translation.